What is claimed is:

Claims:

1. A vertical semiconductor device structure, comprising:

a substrate defining a substantially horizontal plane;

a gate electrode projecting vertically from said substrate;

at least one semiconducting nanotube extending vertically through said gate electrode between opposite first and second ends;

a gate dielectric electrically insulating said at least one semiconducting nanotube from said gate electrode;

a source electrically coupled with said first end of said at least one semiconducting nanotube; and

a drain electrically coupled with said second end of said at least one semiconducting nanotube.

2. The semiconductor device structure of claim 1 wherein said source is composed of a catalyst material effective for growing said at least one semiconducting nanotube.

3. The semiconducting device structure of claim 1 wherein said drain is composed of a catalyst material effective for growing said at least one semiconducting nanotube.

4. The semiconductor device structure of claim 1 further comprising:

an insulating layer disposed between said drain and said gate electrode for electrically isolating said drain from said gate electrode.

5. The semiconductor device structure of claim 1 further comprising:

an insulating layer disposed between said source and said gate electrode for electrically isolating said source from said gate electrode.

6. The semiconducting device structure of claim 1 wherein said at least one semiconducting nanotube is composed of arranged carbon atoms.

7. The semiconducting device structure of claim 1 wherein said at least one semiconducting nanotube defines a channel region of a field effect transistor having a channel along which current flow is regulated by application of a control voltage to said gate electrode.

8. The semiconducting device structure of claim 1 wherein said at least one semiconducting nanotube is oriented substantially perpendicular to said horizontal plane.

9. The semiconducting device structure of claim 1 further comprising:

a plurality of semiconducting nanotubes extending vertically through said gate electrode.

10. The semiconducting device structure of claim 1 wherein said gate dielectric is disposed on said at least one semiconducting nanotube.

11. A method of forming a semiconductor device structure comprising:

forming a conductive pad on a substrate;

growing at least one semiconducting nanotube extending substantially vertically from the conductive pad between a first end electrically coupled with the conductive pad and a second free end;

electrically insulating the at least one semiconducting nanotube with a gate dielectric;

forming a gate electrode electrically insulated from and overlying the conductive pad with the at least one semiconducting nanotube extending vertically through the gate electrode; and

forming a contact electrically coupled with the second end of the at least one semiconducting nanotube and electrically insulated from the gate electrode.

12. The method of claim 11 wherein electrically insulating the at least one semiconducting nanotube comprises:

encasing the at least one semiconducting nanotube inside the gate dielectric.

13. The method of claim 11 wherein forming the contact comprises:

removing the gate dielectric from the free end of the at least one semiconducting nanotube; and

providing a metal feature operating as said contact.

14. The method of claim 13 further comprising:

forming an insulating layer on the gate electrode; and

recessing the insulating layer to expose the free end of the at least one semiconducting nanotube.

15. The method of claim 11 wherein the at least one semiconducting nanotube is a carbon nanotube and the conductive pad is formed of a catalyst material suitable for growing carbon nanotubes, and growing the at least one semiconducting nanotube further comprises:

exposing the conductive pad to a carbonaceous reactant under conditions effective to incorporate carbon atoms into the carbon nanotube with a semiconducting molecular structure.

16. The method of claim 11 wherein growing the at least one semiconducting nanotube further comprises:

growing the at least one semiconducting nanotube by a chemical vapor deposition technique.

17. The method of claim 11 wherein the free end of the at least one semiconducting nanotube projects into a metal constituting the contact.

18. The method of claim 11 wherein the at least one semiconducting nanotube is characterized by arranged carbon atoms.

19. The method of claim 11 wherein the at least one semiconducting nanotube defines a channel region of a field effect transistor having a channel regulated by application of a control voltage to the gate electrode.

20. The method of claim 11 wherein forming the gate electrode comprises:

applying an insulating layer on the conductive pad;

applying a conductive layer overlying the insulating layer; and

patterning the conductive layer to define the gate electrode.

21. The method of claim 20 wherein forming the contact comprises:

recessing the insulating layer to expose the free end of the at least one semiconducting nanotube.

22. The method of claim 21 further comprising:

removing the gate dielectric from the free end of the at least one semiconducting nanotube; and

providing a metal feature operating as said contact.

23. The method of claim 11 wherein said at least one semiconducting nanotube defines a channel region of a field effect transistor having a channel along which current flow is regulated by application of a control voltage to said gate electrode.

24. The method of claim 11 further comprising:

growing at least one conducting nanotube extending substantially vertically from the conductive pad; and

destroying the at least one conducting nanotube before forming the gate electrode.

25. A semiconductor device structure, comprising:

a substrate defining a substantially horizontal plane;

a conductive first plate disposed on said substrate,

at least one nanotube projecting vertically from said first plate and electrically coupled with said first plate;

a conductive second plate positioned vertically above said first plate; and

a dielectric layer electrically isolating said second plate from said first plate and said at least one carbon nanotube.

26. The semiconductor device structure of claim 25 wherein said at least one nanotube has a conducting molecular structure.

27. The semiconductor device structure of claim 25 wherein said at least one nanotube has a semiconducting molecular structure.

28. The semiconducting device structure of claim 25 wherein said dielectric layer defines a coating that encases said at least one nanotube.

29. A method of forming a semiconductor device structure comprising:

forming a conductive first plate on a substrate;

growing at least one nanotube extending substantially vertically from the first plate that is electrically coupled with the first plate;

covering the at least one nanotube and the first plate with a dielectric layer; and

forming a second plate overlying said first plate that is electrically insulated by the dielectric layer from the at least one nanotube and the first plate.

30. The method of claim 29 wherein said at least one nanotube has a conducting molecular structure.

31. The method of claim 29 wherein said at least one nanotube has a semiconducting molecular structure.

32. The method of claim 29 wherein covering the at least one nanotube and the first plate comprises:

encasing the at least one nanotube inside the dielectric layer.